### Session Summary: Supporting Real-time Applications with Ethernet

Rapporteur: Ferdy Hanssen

#### 1. Introduction

This section consisted of four presentations, each lasting ten minutes and each followed by five minutes of questions and discussion. Each presentation and its subsequent discussions is dealt with in a separate section below.

## 2. SBM protocol for providing real-time QoS in Ethernet LANs

Presented by: Anis Koubaa

A performance evaluation was presented of a solution to handle QoS requirements over a LAN using an RSVP-based protocol, called SBM. The presentation first showed an overview of SBM, followed by a performance evaluation of the bandwidth reservation, and finally an evaluation of the recovery time after a failure in the bandwidth manager was shown. One question was raised:

**Question.** The computation of virtual time is not exactly light-weight, how much overhead is introduced by Weighed Fair Queuing?

**Answer.** There is not much overhead introduced. This can be demonstrated when you look at routers in use today, which use the WFQ technique.

# 3. Deadline First Scheduling in Switched Real-Time Ethernet – Deadline Partitioning Issues and Software Implementation Experiments

Presented by: Hoai Hoang

An asymmetric deadline partitioning was presented to allow substantial utilisation increases. The presentation first explained the network architecture and real-time traffic handling assumed, followed by an explanation of asymmetric deadline scheduling. Three questions were raised:

**Question.** Why use Earliest Deadline First scheduling? **Answer.** Because the deadline of tasks is most important in industry.

**Question.** Does you system also allow non-real-time traffic?

Answer. Yes, it does.

**Question.** How much do you delay non-real-time traffic when real-time traffic is currently using the network? **Answer.** Non-real-time traffic may pass when there is no real-time traffic, and the system supports at least 20% of the total bandwidth for non-real-time use.

### 4. Designing, Modelling and Evaluating Switched Ethernet Networks in Factory Communication Systems

Presented by: Eric Rondeau

Methods to design and evaluate switched Ethernet architectures were presented, based on respectively genetic algorithms and the network calculus. The presentation first showed the switch model and how to calculate the maximum end-to-end delay of a switched network, followed by an evaluation method to minimise this end-to-end delay, and finally a design method for switched networks using genetic algorithms was shown. Two questions were raised:

**Question.** How to avoid finding a partial optimum, which is not the overall optimum?

**Answer.** We do not use a random starting point, but a starting point which has been intelligently chosen to avoid such problems.

**Question.** How do you calculate the number of switches with a certain number of ports needed for your network? **Answer.** The number of connections supported depends on the time cycle of the system, the number of ports per switch and the packet bandwidth for all ports per switch. So the number of connections needed, combined with the depth of the star topology of the network and the number of ports per switch can be used to compute the number of switches needed.

## 5. Real Time on Ethernet using off-the-shelf Hardware

Presented by: Jork Löser

A model and implementation of an adaptation at the network level were presented, which provide real-time communication to applications using UDP/IP on standard hardware. The presentation first showed the principle of operation, followed by an explanation of the implementation and results of latency measurements. Two questions were raised:

**Question.** Is the IPC tied into your system?

**Answer.** IPC is included in the system as a component of the microkernel, so it can be ported to other systems or replaced by another protocol relatively easily.

**Question.** What is the difference of your system, compared to commercially available switches?

**Answer.** Our system is not a switch, it is a traffic shaper at the driver level of the operating system.